WHAT IS CLAIMED IS:

1   1.   An electronic device testing system comprising:

2   a tester operable to generate test data and apply the test data to the electronic

3   device to determine the response of the electronic device;

4   a capture interface operable to capture the test data communicated to the

5   electronic device by the tester;

6   a compression engine in communication with the capture interface and

7   operable to compress the test data; and

8   memory in communication with the compression engine and operable to save

9   the compressed test data.

1   2.   The system of Claim 1 further comprising:

2   a de-compression engine interfaced with the memory and operable to de-

3   compress the test data; and

4   an analyzer interfaced with the de-compression engine and operable to analyze

5   the de-compressed test data to determine the test data source of an

6   electronic device error response.

1   3.   The system of Claim 2 wherein the test data comprises plural cycles

2 including empty cycles not associated with the electronic device error response, and

3 wherein the analyzer is further operable to generate a test program that reduces the

4 empty cycles of the test data.

1   4.   The system of Claim 1 wherein the tester is further operable to run the

2 test program on production electronic devices to detect the error response.

1   5.   The system of Claim 1 wherein the tester comprises a vector generator

2 operable to generate vector test data.

1   6.   The system of Claim 5 wherein the electronic device comprises a

2 memory device operable to store data fields according to address and control

3   information and the vector generator generates memory vectors for storage on the

4   memory device.

1   7.   The system of Claim 6 wherein the compression engine further

2   comprises:

3   a compressor having plural comparison modules, each comparison module

4   having a width adapted for comparing data field, address or control

5   information and a depth for comparing predetermined cycles of test

6   vectors, the comparison modules operable to represent test vectors

7   having matching data field, address or control information with a

8   representation having a reduced size to output compressed vectors

9   having variable lengths;

10   a reformater interfaced with the comparison modules and operable to reformat

11   the compressed vectors of the comparison modules as concatenated

12   words of similar length.

1   8.   The system of Claim 7 wherein the compressor further comprises

2   repeating vector detection logic operable to detect repeating test data patterns and to

3   represent the repeating test data patterns as a word having the repeating value and a

4   counter for the number of times the value repeats.

1   9.   The system of Claim 1 wherein the memory further comprises:

2   plural memory motherboards;

3   a memory parser associated with each memory motherboard;

4   plural memory controllers associated with each memory parser; and

5   plural memory storage devices associated with each memory controller;

6   wherein the memory parser coordinates with its associated memory controllers

7   to store test data on plural memory storage devices in sequence so that

8   the memory storage devices operate on a lower clock speed than the

9   test data generation clock speed.

1   10.   A method for testing electronic devices, the method comprising:

2   generating test data for application to the electronic device;

3   communicating the test data to the electronic device through an interface;

4   capturing the test data communicated to the electronic device;

5   compressing the captured test data;

6   storing the compressed test data;

7   detecting an error response by the electronic device to the test data; and

8   analyzing the compressed test data to identify the source of the error response.

1   11.   The method of Claim 10 wherein the electronic device comprises a

2 memory device and generating test data further comprises generating vectors of

3 memory test data for storage on the memory device, the memory test data having data

4 field, address and control information.

1   12.   The method of Claim 11 wherein detecting an error further comprises:

2   reading test data stored on the memory device;

3   comparing the read test data with the test data written to the memory device;

4   and

5   detecting an error if the read test data differs from the written test data.

1   13.   The method of Claim 11 wherein compressing the test data further

2 comprises:

3   comparing the data field, address and control information of a vector with the

4   data field, address and control information of a predetermined number

5   of previous vectors to identify matches in one or more of the data field,

6   address and control information; and

7   representing matches with defined opcodes that reduce the size of the vector.

1   14.   The method of Claim 11 wherein compressing the test data further

2 comprises:

3   detecting repeat patterns; and

4   representing the repeat patterns with the repeated value and a count of the

5   number of repeats of the repeat value.

1   15.   The method of Claim 10 wherein storing the compressed test data

2 further comprises coordinating storage of the test data in plural storage devices so that

3 the storage devices operate at a slower clock speed than the clock speed associated

4 with the generation of the test data.

1   16.   The method of Claim 10 wherein analyzing the test data further

2 comprises:

3   de-compressing the compressed test data to replay the test data applied to the

4   electronic device; and

5   passing the replayed test data through a logic analyzer to determine the applied

6   test data that generated an error response.

1   17.   The method of Claim 16 wherein analyzing the test data further

2   comprises generating a test program to detect the error response by

3   generating test data cycles associated with the error response and

4   reducing test data cycles not associated with the error response.